Synopsis V1.0
HI SEE Test Report for the Samsung 4G NAND Flash Memory

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## I. Introduction

This study was undertaken to determine the susceptibility of the Samsung K9F4G08U0A 4 Gbit NAND Flash memory to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs and for destructive events induced by exposing it to a heavy ion beam at the Lawrence Berkeley National Laboratory Cyclotron facility.

## II. Devices Tested

We tested a total of 3 Samsung K9F4G08U0A 4G NAND devices marked with date code 625. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility. However, we believe that since these devices are fabricated in the still relatively rare 73 nm feature-size technology and were supplied by the manufacturer that their provenance is traceable.

The device technology is 73 nm minimum feature size CMOS NAND Flash memory. The chips came in a 48-pin TSOP package, but the plastic had been dissolved on the topside to expose the chips, allowing the beam to reach the chip surface. The die is shown in Figure 1.

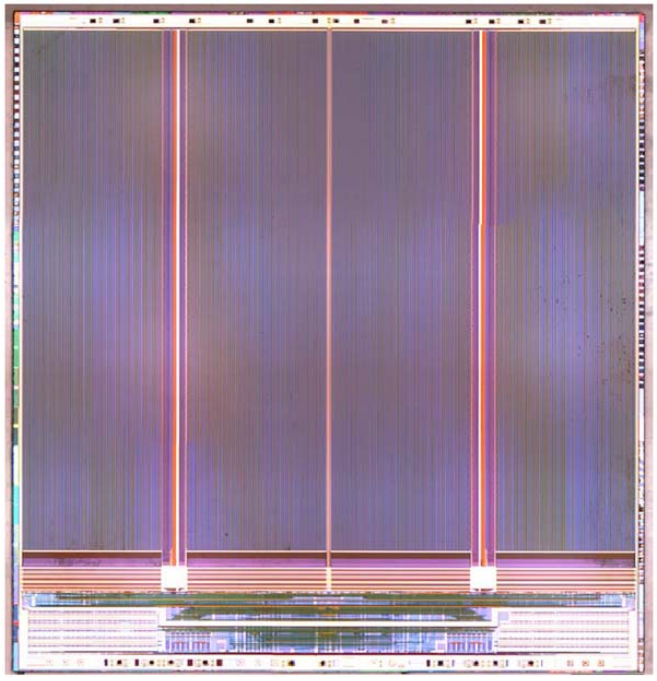


Figure 1. Picture of Samsung K9F4G08U0A chip.

## III. Test Facility

**Facility:** Lawrence Berkeley National Laboratory Cyclotron
**Flux:** (5 x $10^2$ to 1. x $10^5$ particles/$cm^2$/s).
**Fluence:** All tests were run to 1E5 to 1E8 p/$cm^2$, or until destructive or functional events occurred.

Table I: Ions/Energies and LET for this test

| LBNL Ions | Energy/ AMU | Energy (MeV) | Approx. LET on die (MeV•$cm^2$/mg) | Angle | Effective LET |
|---|---|---|---|---|---|
| Ne | 4.5 | 90 | 3.49 | 0 | 3.49 |
| Ar | 4.5 | 180 | 9.47 | 0 | 9.47 |
| Cu | 4.5 | 284 | 21.0 | 0 | 21 |
| Kr | 4.5 | 378 | 30.85 | 0 | 30.85 |
| Xe | 4.5 | 581 | 58.7 | 0 | 58.7 |

## IV. Test Conditions

**Test Temperature:** Room Temperature for SEU
**Operating Frequency:** (0-30 MHz).
**Power Supply Voltage:** ( 3.3V+10% for SEL, 3.3V and 3.3V-10% for SEU).

## V. Test Methods

Because Flash technology uses different voltages and circuitry depending on the operation being performed, testing was performed for a variety of test patterns and bias and operating conditions.

Test patterns included all 0's, all 1's, checkerboard and inverse checkerboard. In general all these patterns were used until a worst-case pattern was established, and then testing was conducted using only the worst-case pattern. Most exposures were with all zeroes stored. Between exposures, all patterns were used to exercise the DUT, to verify that it was still fully functional. The maximum clock frequency for these devices was 40 MHz, which is also the frequency used in the dynamic testing.

Bias and operating conditions included:

1) Static/Unbiased irradiation, in which a pattern was written and verified, and then bias was removed from the part and the part was irradiated. Once the irradiation reached

the desired fluence, it was stopped, bias was restored, and the memory contents were read and errors tallied.

2) Static irradiation, which was similar to unbiased irradiation, except that bias was maintained throughout irradiation of the part.

Note that these conditions provide no opportunity to monitor functional or hard failures that may occur during the irradiation.

3) Dynamic Read, in which a pattern was written to memory and verified, then subsequently read continuously during irradiation. This condition allows determination of functional, configuration and hard errors, as well as bit errors.

4) Dynamic Read/Write, which was similar to the Dynamic Read, except that a write operation is performed on each word found to be in error during the previous Read.

5) Dynamic Read/Erase/Write, which again was similar to the Dynamic Read and Read/Write, except that a word in error was first erased and then rewritten. Because the Erase and Write operations use the charge pump, it is expected that the Flash could be more vulnerable to destructive conditions during these operations.

The Block diagram for control of the DUT is shown in Figure 2. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the FLASH is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for overcurrent conditions and shuts down power to the DUT if such conditions are detected. The test boards are shown in Figure 3.

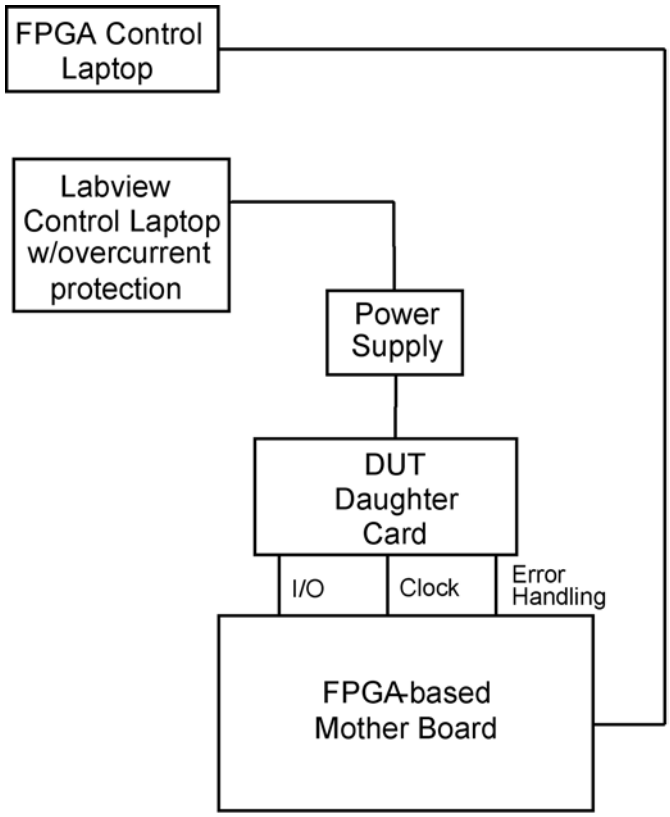
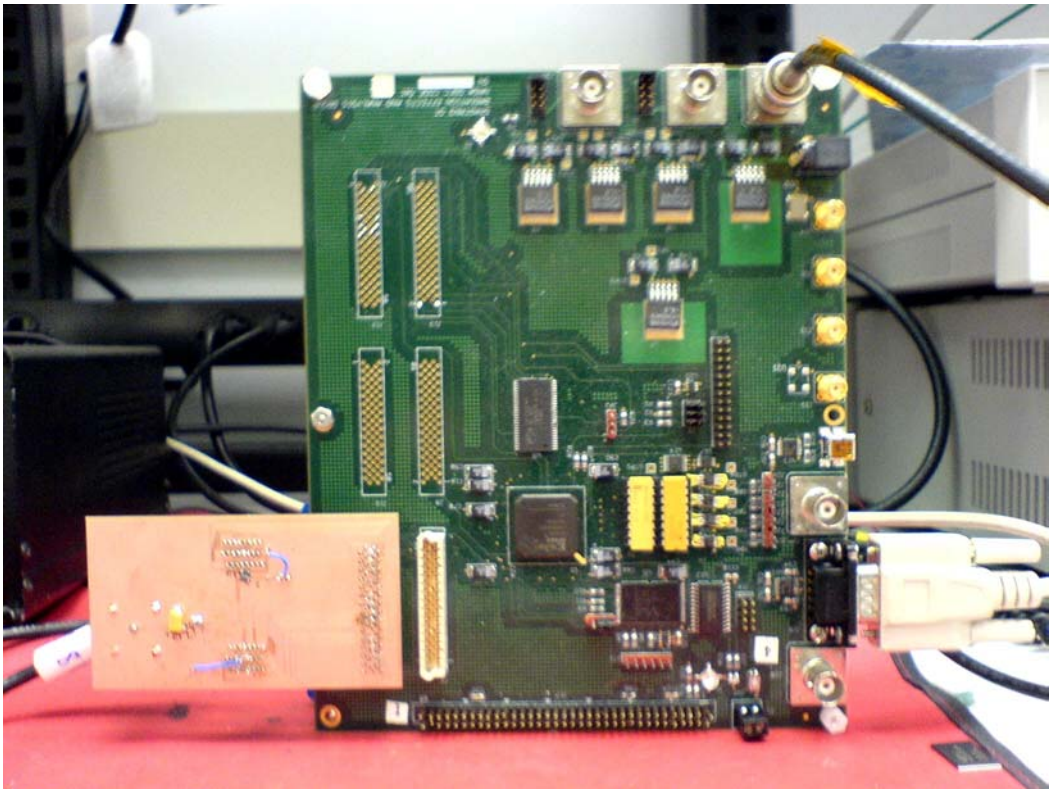
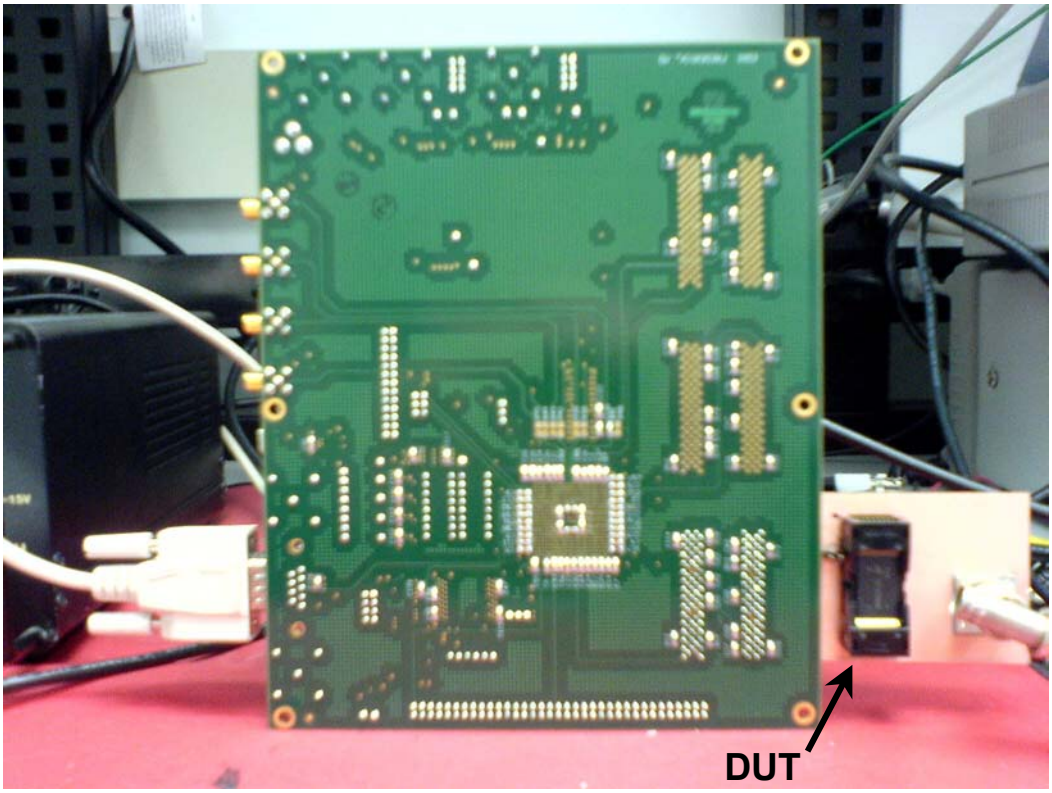



Figure 2. Overall Block Diagram for the testing of the Samsung NAND Flash.



(a)




(b)

Fig. 3. Pictures of test board. (a) front of mother board, (b) front of daughter board, showing DUT.

## VI. Results

During testing, the K9F4G08U0A was irradiated with the ions indicated in Table I. The DUT was oriented normal to the incident beam. The errors observed in static testing are shown in Figure 4. In all cases, the All-0's was found to be the worst-case pattern, so after the first few runs, all subsequent runs were carried out with this pattern.

Even for the static case, bit errors and Page/Block errors were evident in the patterns of upsets observed. It is likely that the Page/Block errors arise due to upsets in configuration registers in the memory array. Because the rate at which errors came in could not be gauged, we could not determine exactly when a page/block error occurred, so cross sections are approximate for these error modes. Here and in the following discussion, bit errors are taken to be single bits, which are flipped, as a result of the interaction with incident ions, normally from zero to one. We do not have the physical to logical address mapping, which would allow us to look for multiple bit errors (error clusters) for these parts. However, in the overwhelming majority of cases, there is only one error in a page, or one error in an entire block, which makes it extremely unlikely that there will be multiple errors from a single ion. This result is consistent with previously published results on the upset mechanism in flash memory—an ion passing through a floating gate creates a dense charge column, which creates a conducting path between the gate and substrate, which allows charge to leak off the floating gate. Since the ion only hits one gate, only one bit is affected. This situation is far different from that in volatile memories, where charge generated in the Si substrate can be shared across multiple nodes. The only apparent multiple bit errors are cases where an entire page or a block (or a large part of one) upsets simultaneously—these page and block errors are attributed to errors in the control logic, rather than to the individual bits. These are counted as SEFIs (Single Event Functional Interrupt). In general, a SEFI is any event where the entire DUT, or a large part of it, stops working, presumably from an interaction with a single ion. As a practical matter, most of the SEFIs recorded here are either page errors or block errors, although a few involve multiple pages or multiple blocks.

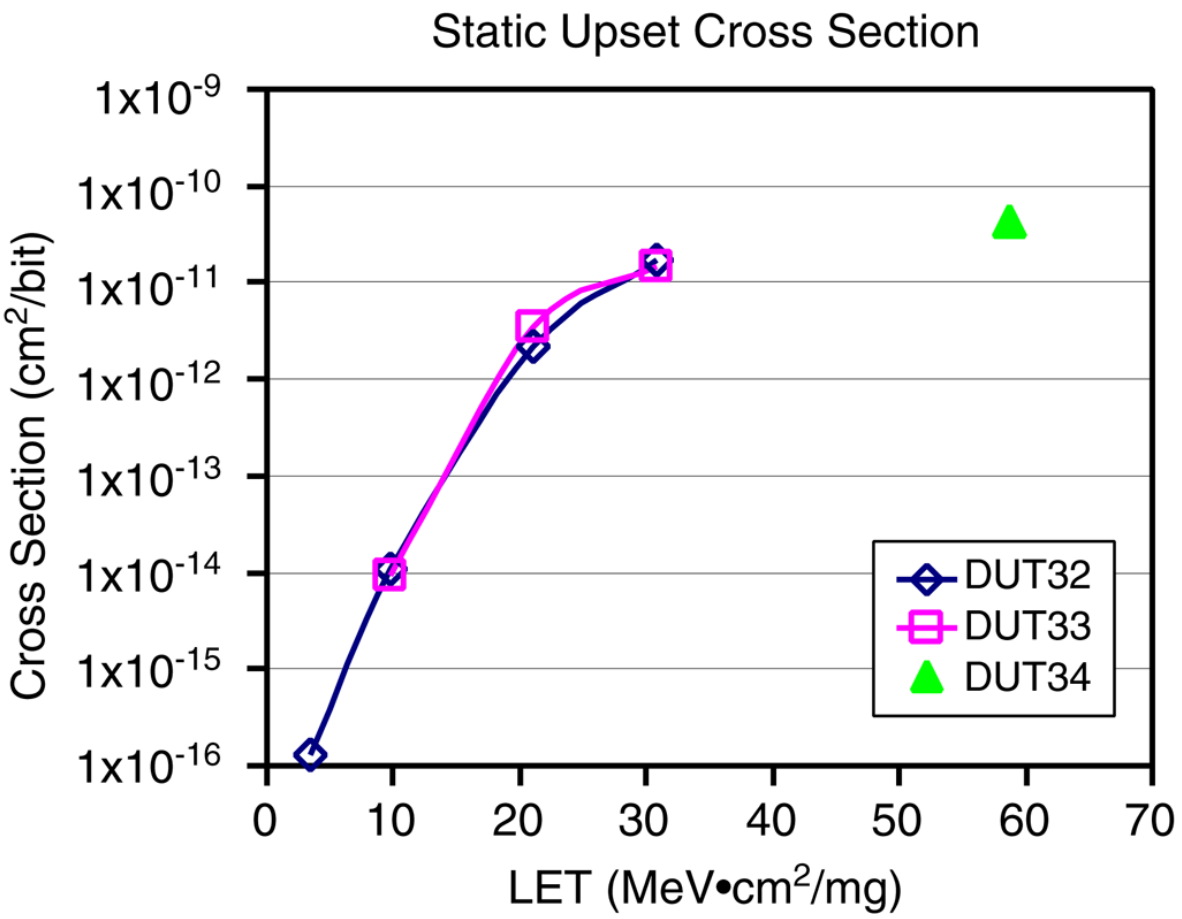



Figure 4. Error cross-sections observed in static testing.

The results in Figure 4 were fitted with Weibull parameters, threshold LET=3.5, saturation cross section=5E-11 $cm^2$/bit, width=27, exponent=5, and Creme96 was used to calculate the bit error rate for geosynchronous orbit at solar minimum. The result was 1E-12 errors/bit-day, which is equivalent to about 1.5 bit errors per year for a 4G. The data in Figure 4 is replotted in Figure 5, normalized per device, instead of per bit, so that the SEFI and destructive effects can be shown on the same scale. Obviously, the SEFI and destructive error cross sections are much less than the bit upset cross section, and the error rate expected in space will scale with the cross section. However, we have not calculated this error rate, because there are so few SEFI or destructive events that there is large statistical uncertainty associated with them.

For the Dynamic Read condition, the parts showed exhibited transient read errors in addition to the bit and Page/Block errors. For Dynamic Read/Write and Dynamic Read/Erase/Write, functional failures were observed that made it impossible to Erase or Write to the memory. Page/Block and SEFI errors were also identified in some cases, but others may have been lost due to functional failure of the chip. For these test modes, results are shown in Figures 6-8.

All the testing was done at room temperature, which is not a worst-case condition for SEL (single event latchup). However, we did monitor the DUTs for SEL, and there were seven shots where a high current state was observed—current was monitored as a function of time throughout all the exposures. All the DUTs drew 3-4 mA before the beam was turned on. In these seven shots, it was common for the current level to fluctuate—3 mA to 8mA, back to 3,

then to 18 or 30, then 8 mA again, sometimes back to 3 mA, etc. This kind of result suggests a localized micro-latch or some kind of bus contention. A generalized latchup condition would not be expected to correct itself. Only one shot produced results, which could indicate true latchup, but even there the results are unclear. The current had fluctuated between about 3 and 18 mA for most of the exposure time, but it increased to about 150 mA for about half a second, before settling back to 100 mA (100 mA is the current limiting level). The current was then steady at that level until the end of the exposure, about 15 seconds later. On one other shot, the current went up to 160 mA, before settling back to the current limiting level. But on the second shot, it only held at 100 mA for about two seconds, before dropping to 33 mA. At that point, the test engineer intervened, and cycled the power. But on other shots, the DUT had recovered without intervention from current levels of approximately 30 mA. It is possible that, on the one shot where the current did not recover, it would have recovered if there had been more time before the end of the exposure. Therefore, we conclude that there was only one possible latchup, but even that is ambiguous. If it was a latchup, it was nondestructive. This shot is plotted (as a SEFI, which is not ambiguous) in Fig. 5. A SEFI was observed on every high current shot. Plots of the power supply current are shown for two shots, in Figure 9 and Figure 10. These are the two shots where the current goes up to the current limit, 100 mA. In Figure 9, the current partially recovers spontaneously; in Figure 10, it does not.

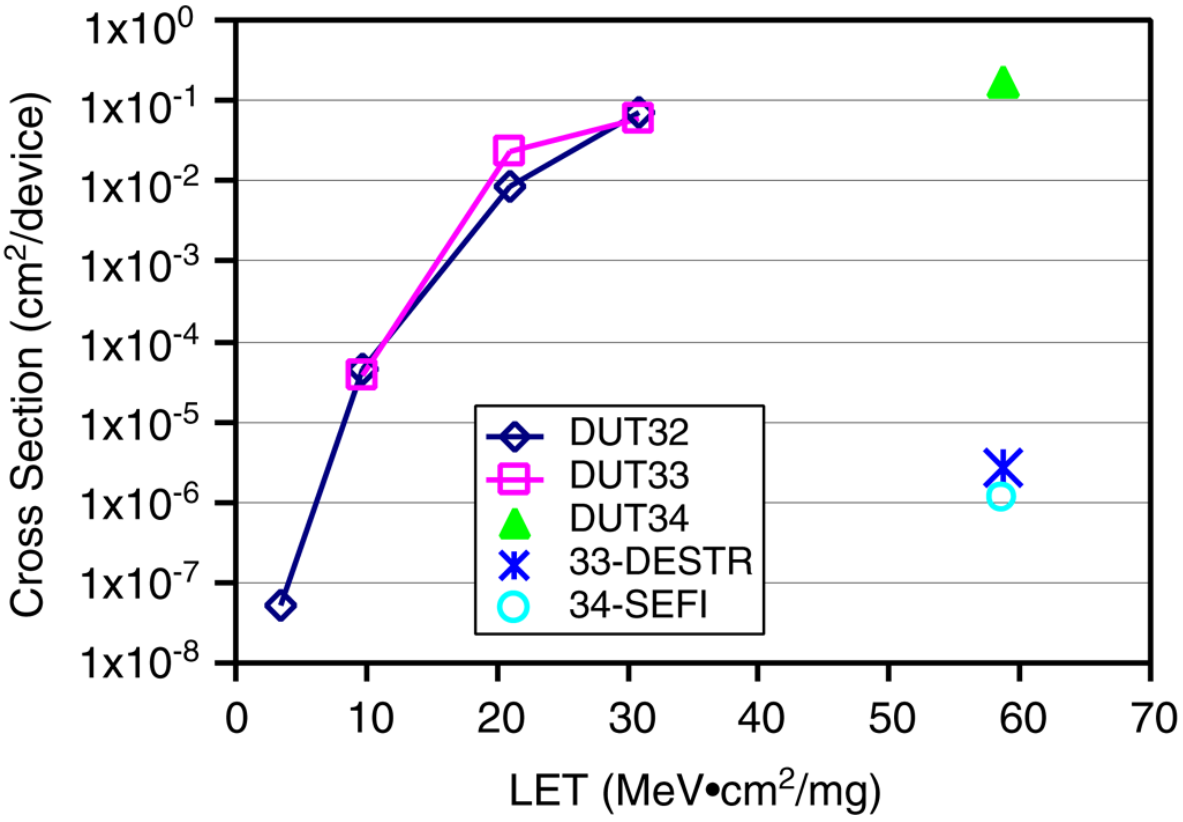



Fig. 5. Static upset cross sections.

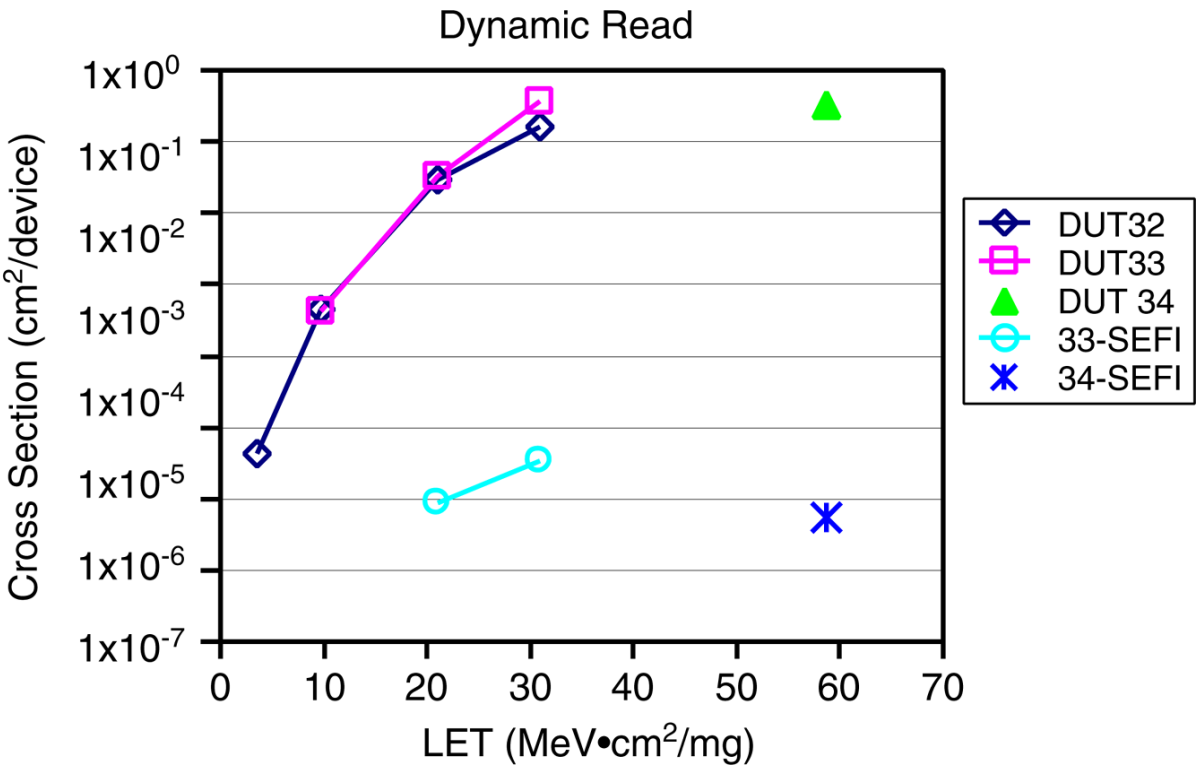



Fig. 6. Dynamic read upset cross section.

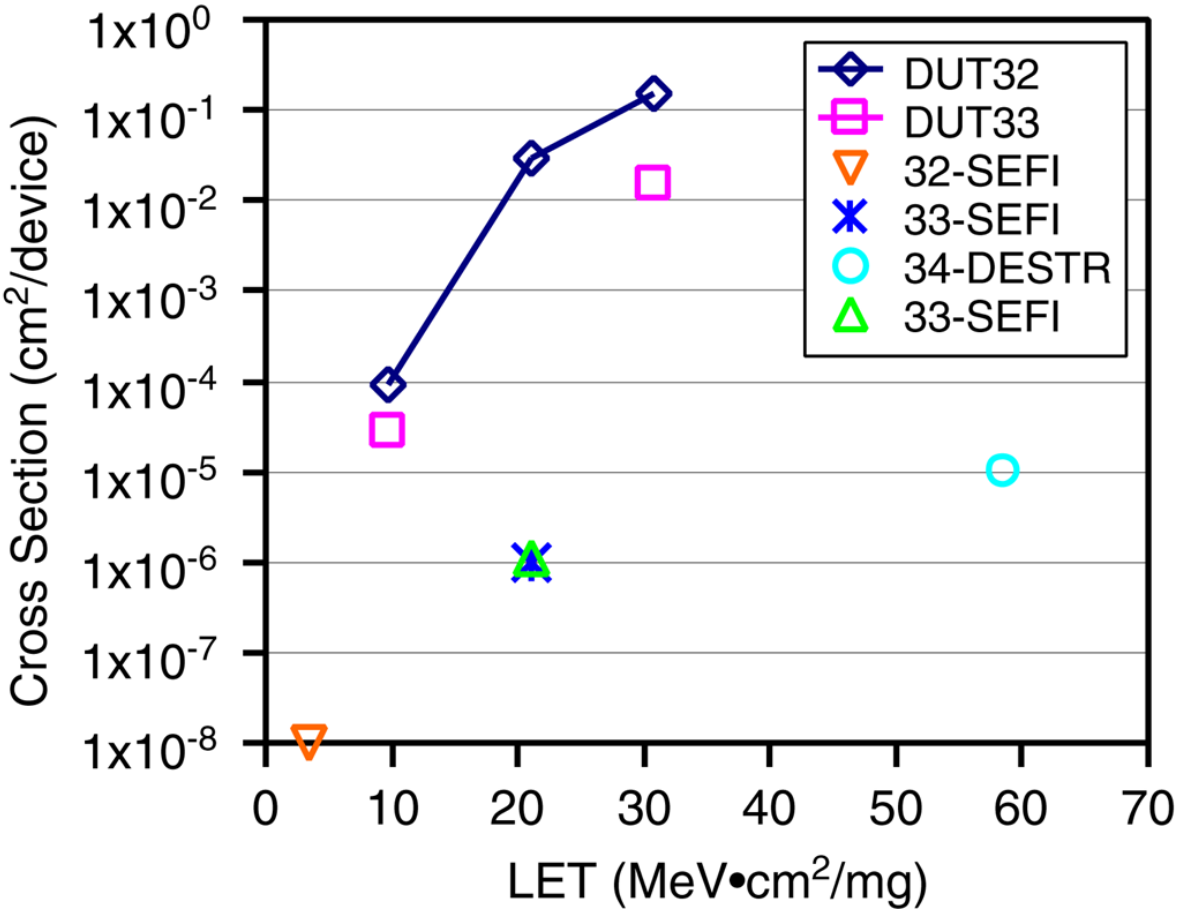



Fig. 7. Error cross sections observed in dynamic read/write testing.

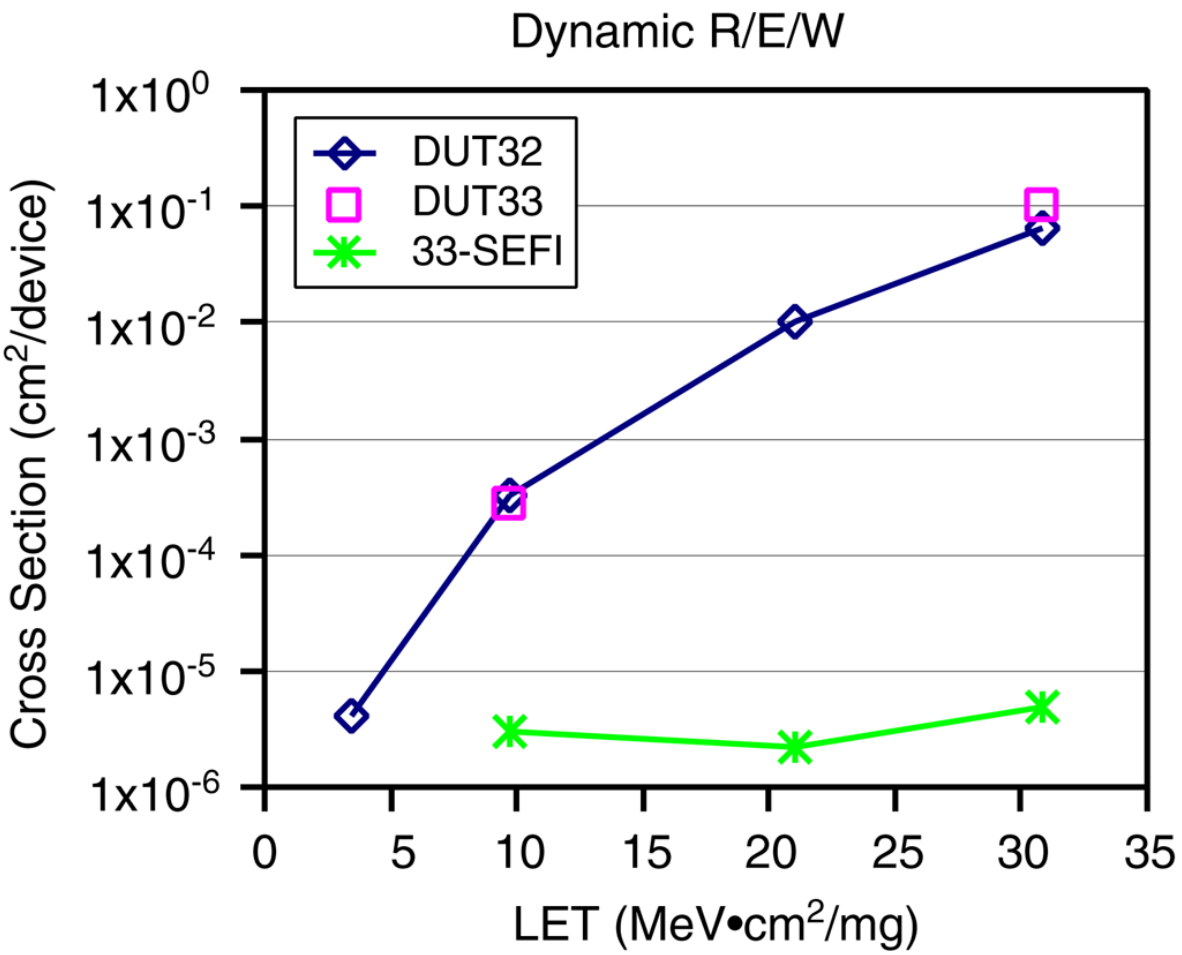



Fig. 8. Error cross sections observed in dynamic Read/Write/Erase testing.

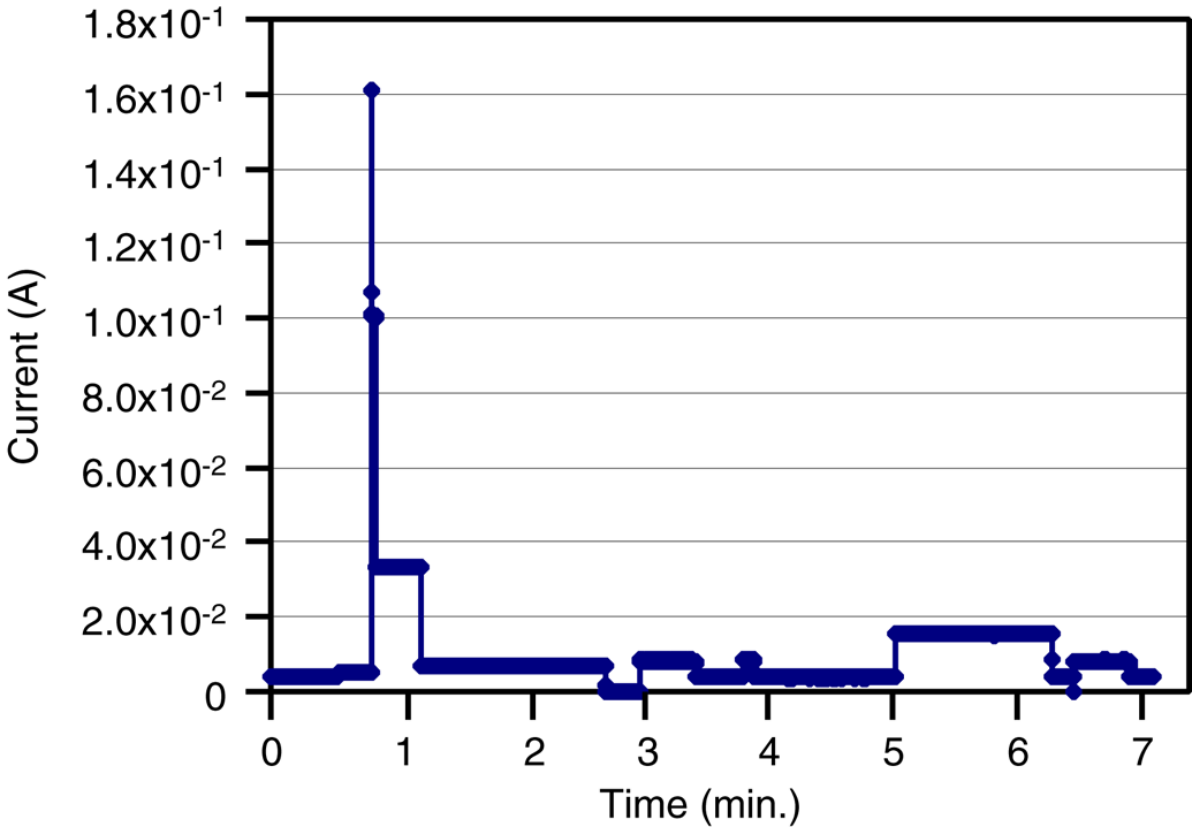



Fig. 9. Current vs Time, no latchup.

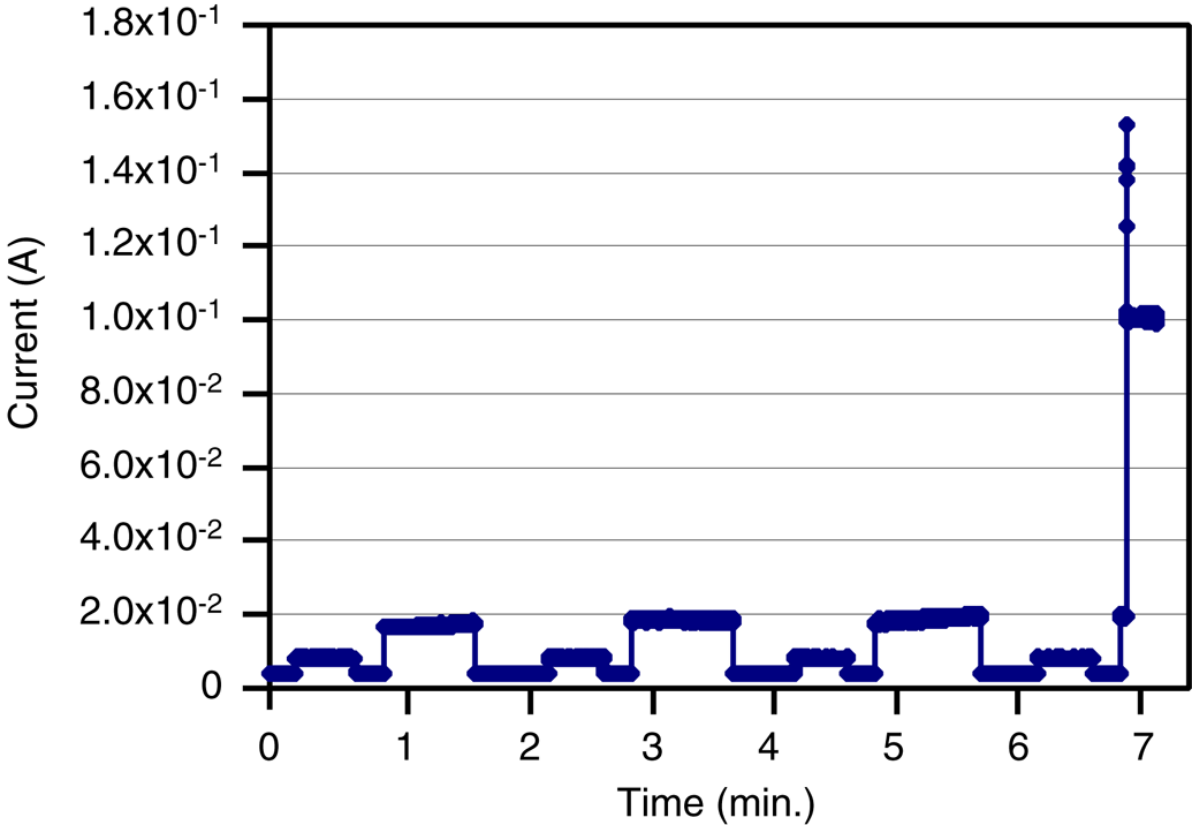



Fig. 10. Current vs Time, possible latchup.

## VII. Recommendations

The Samsung K9F4G08U0A 4 Gbit NAND Flash memory has TID tolerance above 100 krad ($SiO_2$), as reported previously, which makes it suitable for some NASA missions. The static bit error rate, reported here, is low enough to make the technology very attractive for some NASA missions. However, the SEFIs observed, require mitigation strategies that have not been worked out yet. Whether or not the technology is suitable for a specific mission depends on the mission requirements.

## VIII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Samsung K9F4G08U0A. Additional testing is required before these devices can be considered for space applications. SEFIs will need to be better understood, and mitigation strategies identified.

In prior TID testing, these devices showed some promise for applications with moderate dose levels. Additional TID testing is recommended to fully characterize TID degradation.